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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/675,776	DEWITT ET AL.	
	Examiner	Art Unit	
	Tuan A. Vu	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 June 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/27/07; 6/26/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to the Applicant's response filed 6/06/07.

As indicated in Applicant's response, claims 1, 4, 10, 13, 16, 18, 21, 24-25 have been amended. Claims 1-25 are pending in the office action.

Information Disclosure Statement

2. The resubmitted IDS has been considered; however, it is urged that Applicants revise any Disclosure Statement material being submitted in the future in order to show some amiable effort that would otherwise alleviate the Examiner's burden when non relevant subject matter is provided in extraneous abundance.

Double Patenting

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claims 1, 13, 21 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 3, 20, 25 of copending Application No. 10/675777 (hereinafter '777).

Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following observations.

As per instant claims 1, 13, 21, '777 claims 3, 20, 25 also recite determining for a instruction during execution for a association of an indicator; associating a counter based on such determination and incrementing a counter in response to the indicator association with the instruction. The event counting as recited by '777 is construed as obvious representation to a runtime indicator (leading to a counter increment, in which incrementing is count of number of instructions execution) of the instant claims.

5. Claims 1, 13, 21 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 9, 19, 23, 25 of copending Application No. 10/675778 (hereinafter '778). Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following observations.

As per claims 1, 13, 21, '778 claims 1, 9, 19, 23, 25 recites an execution environment wherein upon determining that an indicator (Note: even though '778 does not recite indicator per se, a threshold exceeding point can be conceived as a runtime indicator) is associated with an instruction, counting execution of such instruction based on such indicator. Even though '778 recites that the indicator is a threshold value event, this limitation would be a obvious representation of any runtime indicator that would characterizes as an event deemed for the counter to be incremented -- in which incrementing is count of number of instructions execution -- in view of the above association.

6. Claims 1, 13, 21 and 10, 18, 25 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 2, 16 of copending Application No. 10/675872 (hereinafter '872).

As per instant claims 1, 13, 21, '872 claims 2, 16 also recite determining whether an instruction in execution is related with an runtime 'indicator' (Note: even though '872 does not recite indicator per se, a point in a memory range can be analogous to a runtime indicator); and counting each event associated with the instruction if the instruction is associated with that indicator. Even though '778 recites that the indicator is a point in contiguous range, this limitation would be a obvious representation of any runtime indicator that would characterizes as an event deemed for the counter to be incremented (in which incrementing is in terms of count of number of instructions execution) in view of the above association.

As per instant claims 10, 18, 25, '872 claims 2, 16 also recite determining whether a memory access instruction is associated with a 'memory location' (Note: even though '872 does not recite memory location per se, a point in a memory range can be analogous to a location); and counting each event associated with the instruction if the instruction is associated with that determination. Even though '872 explicitly recites that the indicator is a location within contiguous range, this location-within- range limitation would be a obvious representation of any runtime indicator that would characterizes as an event deemed for the counter to be incremented (in which incrementing in terms of count of number of instructions execution) in view of the above association determination.

7. Claims 1, 13, 21 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 9, 17 of copending Application No. 10/675721 (hereinafter '721).

As per instant claims 1, 13, 21, '721 claims 1, 9, 17 also recite determining for a instruction during execution for a association of a indicator (Note: even though '721 does not

recite an indicator per se, a set of indicators can be analogous to one such runtime indicator) ; incrementing a counter in response to the indicator association with the instruction. The instruction in the *routine of interest* as recited by '721 is construed as obvious representation to a runtime instruction that requires some action (e.g. to monitor or to trace/modify leading to a counter increment in which incrementing is in terms of count of number of executions) of the instant claims.

8. Claims 10, 18, 25 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 9, 17 of copending Application No. 10/682385 (hereinafter '385).

As per instant claims 10, 18, 25, '385 claims 1, 12, 23 also recite determining whether a memory access instruction is associated with a indicator (Note: even though '385 recites data values in memory specifying counting event, a runtime event such as those memory indicators can be analogous to on runtime indicator of the instant claim); and counting each event associated with the instruction if the instruction is associated with that memory location in view of the indicator. Even though '385 explicitly recites that counting events associated with execution based on detection of value indicators, this limitation would be a obvious representation of any runtime indicator that would characterizes as an event deemed for the counter to be incremented (in which incrementing is in terms of count of number of executions) in view of the above association determination.

Claim Objections

9. Claims 1, 13, 21 are objected to because of the following informalities: the phrase recited as 'contains an indicator' does not seem to be a proper construct to describe what is

described in the Specifications. According to which, the structure of Figure 5 is implemented into slots containing the instructions of a given subroutine, and a template slots for storing indicator bits. The related text at pages 26-27 for loading the bundle of instruction into a cache disclose reading of those indicators to have them sent to a performance monitoring unit. The instruction by itself does not contain (emphasis added) any indicator, because the indicator is stored in a template structure adjacent to the row destined for the subroutine's instruction slots, the indicators only there to associate the instructions for a runtime monitoring. The above improper use language will be treated as though the indicator as contained in a structure solely to associate execution event of some instruction with the runtime monitoring or a counter unit.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

10. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

11. Claims 1-9, 13-17, 21-24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The limitation recited as '... instruction ... contains an indicator' (re claims 1, 13, 21) has no reasonable support from reading the corresponding text in the Specifications; and this has been analyzed in the above Claim Objections. That is, one of skill in the art would not be able to understand how the bundle described in Figure 5 and the indicator bits inside a *template* built adjacent to the row of instructions of such bundle can (in view of the above limitation) be equated to a teaching that the indicator are **contained inside** one of those instruction.

Architecture of a computer is a fixed hardware being designed to accommodate a specific instruction within the confined architecture hardware; and one of skill in the art can not see how such instruction can suddenly contain extra bits when the Disclosure does not explain how a architectural instruction is modified to include some non-architectural bit or field. The limitation as identified above is rendering the true capability of the invention all the more obscure. For lack of specific, deliberate, and credible description, the above limitation will not enable one of skill in the art to make use of the claimed invention; and the limitation will be treated as set forth in the Claims Objections.

Also recommended is that any erroneous part of the Disclosure in regard to using the above language (*contains ... indicator*) be modified as well; but this will not be held in abeyance.

Claims 2-9, 14-17, 22-24 are rejected for failing to remedy to the base claims.

Claim Rejections - 35 USC § 102

12. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

13. Claims 1-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Gover et al., USPN: 5,752,062(hereinafter Gover)

As per claim 1, Gover discloses a method in a data processing system for monitoring execution of instructions, the method comprising: determining whether an instruction contains an indicator (e.g. Fig. 5; *count number, bit fields, MMCRO* - col. 10, lines 31-35; Fig. 6A; col. 11, line 62 to col. 12, line 42) wherein the indicator identifies the instruction or first memory

location as one that is to be monitored by a performance monitor unit (e.g. PMCn 51 - Fig. 4, 6-7); and

incrementing a counter associated with the instruction (e.g. *even... to be recorded/counted, counter ... selection, counter freeze* - col. 8, lines 41-50; col. 10, lines 53-63; col. 11 lines 14-50) in response to detecting execution of the instruction and to a determination that the instruction is associated with the indicator, the incrementing providing a count of a number of times the instruction was executed (e.g. Fig. 3: FINISHED ; *number ... branches dispatched ... completed* - col. 20, lines 48-65; *load or store* - col. 22 lines 10-35; Fig. 8).

As per claim 2, Gover discloses resetting the counter if the counter exceeds a threshold value (e.g. *reset* - col. 12, lines 4-42).

As per claim 3, Gover discloses reading a value of the counter prior to the counter exceeding the threshold value (e.g. *enabled ... when low ... exception is signaled* – col. 11, lines 29-37 --Note: interrupt based upon exceeding of a number reads on reading a state and a counter value prior to such interrupt event – see col. 9 lines 16-20).

As per claim 4, Gover discloses incrementing the counter (Fig. 2; col. 9, lines 10-56; Fig. 4-5) in response to detecting execution of the instruction and to a determination that the instruction is associated with the indicator.

As per claim 6, Gover discloses wherein the counter is located in a shadow memory (e.g. col. 8, lines 26-39 – Note: special registers with state or content – MMCRn -- maintained via special privilege access mode and being kept in parallel with execution scheduling – see col. 11, lines 14-50 -- as informational support thereof, hence reads on shadowing type of information kept in memory; see SSR col. 9 lines 36-57).

As per claims 5 and 7, Gover discloses wherein the counter is a field (Fig. 6a-b) in the instruction; that the indicator is the counter (Fig. 6a-b; col. 11-12).

As per claim 8, Gover discloses changing the indicator to disable counting (e.g. *user may determine* - col. 10 line 64 to col. 11, line 46; *user selectable* - col. 12, line 59 to col. 13, line 16) execution of the instruction upon subsequently encountering the indicator.

As per claim 9, Gover discloses wherein the determining step (e.g. Fig. 1, 4-5 and related text; col. 11-12; Fig. 6a-b) is initiated when the instruction is executed.

As per claim 10, Gover discloses a method in a data processing system for monitoring access to data, the method comprising:

responsive to an access to a memory location (e.g. *data accesses* – col 10, lines 17-23), determining whether the memory location contains an indicator (e.g. Fig. 3-5; col. 8, lines 26-39; col. 11, lines 14-50) wherein the indicator identifies the instruction or first memory location as one that is to be monitored by a performance monitor unit (e.g. PMCn 51 - Fig. 4, 6-7); and

responsive to the memory location being associated with the indicator, incrementing a counter associated with the memory location (e.g. col. 8, lines 41-50; col. 11-12); the incrementing providing a count of a number of times the instruction was executed (e.g. Fig. 3; FINISHED ;*number ... branches dispatched ... completed* - col. 20, lines 48-65; load or store - col. 22 lines 10-35; Fig. 8).

As per claims 11-12, Gover discloses wherein the counter is located in a field; wherein the field includes a control bit that forms the indicator (e.g. Fig. 6a-b).

As per claim 13, Gover discloses a data processing system for monitoring execution of instructions, the data processing system comprising: determining means for determining whether

an instruction contains an indicator, wherein the indicator identifies the instruction or first memory location as one that is to be monitored by a performance monitor unit; and incrementing means for incrementing a counter associated with the instruction in response to detecting execution of the instruction and to a determination that the instruction is associated with the indicator, the incrementing providing a count of a number of times the instruction was executed;

all of which limitations having been addressed in claim 1.

As per claims 14-17, refer to the corresponding rejection as set forth in claims 2-4, 8 respectively.

As per claim 18, Gover discloses a data processing system in a data processing system for monitoring access to data, the data processing system comprising: determining means, responsive to an access to a memory location, for determining whether the memory location contains an indicator wherein the indicator identifies the instruction or first memory location as one that is to be monitored by a performance monitor unit; and incrementing means, responsive to the memory location being associated with the indicator, for incrementing a counter associated with the memory location, the incrementing providing a count of a number of times the instruction was executed;

all of which limitations having been addressed in claim 10.

As per claims 19-20, refer to the corresponding rejection as set forth in claims 11-12 respectively.

As per claim 21, Gover discloses a computer program product in a computer readable medium for monitoring execution of instructions, the computer program product comprising:

first instructions for determining whether an instruction contains an indicator, wherein the indicator identifies the instruction or first memory location as one that is to be monitored by a performance monitor unit; and

second instructions for incrementing a counter associated with the instruction in response to detecting execution of the instruction and to a determination that the instruction is associated with the indicator, the incrementing providing a count of a number of times the instruction was executed (refer to corresponding rejection as set forth in claim 1)

As per claims 22-24, refer to the corresponding rejection as set forth in claims 2-4 respectively.

As per claim 25, Gover discloses computer program product in a computer readable medium for monitoring access to data, the computer program product comprising: first instructions for determining whether the memory location contains an indicator, wherein the indicator identifies the instruction or first memory location as one that is to be monitored by a performance monitor unit, responsive to an access to a memory location; and second instructions for incrementing a counter associated with the memory location, responsive to the memory location being associated with the indicator, the incrementing providing a count of a number of times the memory location is accessed (refer to corresponding rejection as set forth in claim 10; *load or store* - col. 22 lines 10-35).

Response to Arguments

14. Applicant's arguments filed 6/06/07 have been fully considered but they are not persuasive. Following are the Examiner's observation in regard thereto.

35 USC § 102 Rejection:

(A) Applicants have submitted that Gover discloses monitor mode control register is incremented based on event occurrence; and this register by Gover (Fig. 6A-B) is not a instruction identified by an indicator as currently redefined in claim 1 (Appl. Rmrks pg. 13, middle). The language recited as 'indicator identifies the instruction or a first memory location ... that is to be monitored by a performance monitor unit' has been dissected and preliminarily construed along with 'counter associated with the instruction ...' as in the following:

(i) a performance monitor unit (PMU) monitors a location or an instruction;

(ii) such location or instruction is being identified by some indicator **contained in** a instruction;

(iii) a counter being associated with the instruction is incremented.

The claim as it is recited has its flaws in terms of lack of definiteness; and reasonable teaching leading to a more or less manageable practical application.

One would ask what the structural relationship between the counter and the instruction amounts to in terms of establishing how this counter can be construed as anything related to the instruction, to the monitor unit, and even to the indicator. The only structural insight is that the indicator resides in the instruction whereby the instruction can be monitored by some unit. But from the lack of relationship between the counter and the monitoring by the PMU, one would be hard pressed to reckon that a counter is this very instruction being monitored by the PMU by way of some indicator integral to the instruction. Based on the lay out of (i) (ii) and (iii) and the missing relationship among them, it is impossible to give weight to the above argument. And harder it would be to accept how Gover's register is suddenly required to be analogized with an instruction (in the line of Applicants' assertion) when the claim does not establish a clear

teaching to preclude the use of Gover's bit fields to support a monitoring count when an instruction event occurs. When the claim does not establish the relationship between the elements recited, broad interpretation has been used. Accordingly, the indicator is merely interpreted as an indicator stored somewhere in memory to support an instruction monitoring process, whereby a count can be incremented in response to the indicator indicating an (instruction) event. And this interpretation has its reasonable stead without reading the Specifications or with considering the Specifications; i.e. if the Specifications were to be imported into the claim.

In light of the invention Specifications, the so-called indicator amounts to some field or bits being stored in a template, associated with a bundle or structure containing the template, the structure representing a subroutine with distinct slots of instructions, the bundle being loaded in a instruction cache; and that loading at runtime sends this indicator value inside said structure template to the PMU. The indicator as disclosed is not contained in any instruction for they are there stored in a common structure with the instruction slots to **associate** runtime events about the instructions; and this teaching is rendering the phrase 'instruction contains an indicator' a misphrased teaching, as set forth in the USC § 112 rejection. The above indicator has been treated as some indicator stored external to the instruction and destined to be read to support a performance-monitoring unit whereby a count is incremented; and accordingly, Gover has been deemed fulfilling the claim (refer to rejection). There is no direct obligation between a counter being incremented and the indicator as claimed; nor is there any teaching that would force that a register bit cannot be an indicator being integral to the very instruction, to enforce that a MMC bit (by Gover) being indicative of a count (associated with execution event) is precluded from

anticipating the incrementing step or the indicator limitation. Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references.

(B) Applicants have submitted that Gover's monitor mode control register --which is used to control a counter -- cannot be an instruction as required by the claims (Appl. Rmrks pg. 14, top and middle). In reply, there are no specifics in the claim that enforce that the indicator used to associate an instruction for its runtime monitoring has to be **the** instruction itself; and if it were, the Specifications would be considered utterly insufficient to corroborate to such concept. The argument appears to fall back into the ambit of the issues and observations made in section A; hence is not persuasive because the language of the claim in light of the Claims Objections and § 112 Rejection is far from supporting the argument.

The argument is not sufficient to overcome the rejection.

(C) In light of the above, the claims will stand rejected as set forth in the Office Action.

Conclusion

15. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan A Vu whose telephone number is (571) 272-3735. The examiner can normally be reached on 8AM-4:30PM/Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571)272-3756.

The fax phone number for the organization where this application or proceeding is assigned is (571) 273-3735 (for non-official correspondence - please consult Examiner before using) or 571-273-8300 (for official correspondence) or redirected to customer service at 571-272-3609.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuan A Vu
Patent Examiner,
Art Unit 2193,
July 29, 2007